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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,746	01/12/2004	Qi Xiang	039153-5003 (G0167)	9599

34083 7590 02/22/2006

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EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/755,746	XIANG, QI	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5,13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/26/05;1/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This is in response to the amendment filed 10/22/05.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-4, 6-12, and 17-20 in the paper filed 10/20/06 is acknowledged.

2. Claims 5 and 13-16 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in paper filed 10/20/05.

The applicant requested reconsideration of the restriction, but did not state there was a traversal, nor set forth arguments as to why the restriction may have been in error. Therefore, the election is considered to be without traversal.

Priority

3. This application claims priority to application 10/341683. However, 10/341683 is directed toward stem cells, not integrated circuits and is a separate inventorship. The applicant is requested to submit all papers necessary to correct this error.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-3 and 9-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 and 9-11 of U.S. Patent No. 6,673,696. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is obvious that the silicon nitride layer of 6,673,696 is a mask layer.

6. Claims 1-3 and 9-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 and 9-11 of U.S. Patent No. 6,292,857. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is obvious that the silicon nitride layer of 6,292,857 is a mask layer.

7. Claims 1-3 and 9-11 and 17-18 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over

claims 21-23 and 28-30 and 36-37 of copending Application No. 10/389456. Although the conflicting claims are not identical, they are not patentably distinct from each other because the independent claims of 10/389456 additionally recite a temperature limitation.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-2, 6, 8, and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Comfort (US005266813A).

Comfort teaches all of the positive steps of claims -2, 6, 8, and 17-18 as follows.

Regarding claim 1, Comfort forms a mask layer (40) above a substrate including germanium (20), selectively etches the mask layer to form apertures in the mask (figure 2) associated with locations of the trance regions, forms trenches (figure 2), provides a semiconductor material (60) by selective epitaxial growth, and forms oxide liners using the semiconductor layer in the trench (depositing oxide layer 70 on silicon layer 60). Regarding the selective epitaxial growth, Comfort teaches epitaxial deposition (thus

epitaxial growth (column 5 lines 8-10) and that the layer in areas other than exposed silicon does not form single crystal silicon, thus selective and a growth dependent upon the underlying layer. Regarding the plurality of trenches, the summary of the invention teaches that devices are separated by trench structures. Thus any single trench teaching applies to a plurality of trenches.

Regarding claim 2, an insulative material (80) is provided in the trenches to form trench isolation regions.

Regarding claim 6, the semiconductor material includes silicon (column 5 line 11).

Regarding claim 8, the oxide liners are formed in a oxidation process (dielectric layer 70 is deposited over layer 60. deposition of a silicon oxide is an oxidation process.). Comfort teaches that silicon liner 60 can be pasivated by thermal oxidation (column 5 lines 25-31).

Regarding claim 17, Comfort teaches a liner in a trench in a germanium containing layer (20), by selectively etching the germanium containing layer to form the trench (figure 2), provides a semiconductor material (60) by selective epitaxial growth, and forms oxide liners from the semiconductor layer in the trench (depositing oxide layer 70 on silicon layer 60). Regarding the selective epitaxial growth, Comfort teaches epitaxial deposition (thus epitaxial growth (column 5 lines 8-10) and that the layer in areas other than

exposed silicon does not form single crystal silicon, thus selective and a growth dependent upon the underlying layer. Comfort teaches that silicon liner 60 can be pasivated by thermal oxidation (column 5 lines 25-31).

Regarding claim 18, Comfort teaches the semiconductor layer may be formed by UHVCVD (column 5 line 10) and that that process is preformed at a temperature below 600C. (column 4 lines 5-10).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos (US006136664A) in view of Van Zant (pages 31 and 39).

Economikos teaches all of the positive steps of claims 1-3, 6-8 except for the use of a substrate containing germanium.

Regarding claim 1, Economikos teaches a silicon substrate (column 4 line 10). The term "silicon substrate" generally refers to a substrate containing silicon, but is not limited to pure silicon. Van Zant teaches that silicon and germanium are both common substrate

materials (page 31) giving them an art recognized equivalence for substrate material. Further, Van Zant teaches the use of silicon-germanium substrates as producing a faster chip (page 39).

Economikos teaches a mask (layers 10 and 15), selectively etching the mask layer to form apertures (45), forming trenches (47) at the location of the apertures by selectively etching the substrate, providing semiconductor material within the trenches and forming an oxide liner using the semiconductor layer (column 4 lines 25-30) by an oxidation process (column 4 lines 25-26).

Regarding claim 2, Economikos provides an insulative material by oxidizing the silicon.

Regarding claim 3, the insulative material is removed to expose the mask (column 4 lines 30-34).

Regarding claim 6, the semiconductor material is silicon (column 4 lines 20-21).

Regarding claim 7, a silicon nitride layer (50) is provided above the substrate and an amorphous capping layer (60) is provided above the silicon nitride layer.

Regarding claim 8, the oxide liners are formed in a oxidation step (column 4 line 54).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Economikos to use a silicon-germanium substrate as taught by Van Zant to provide a faster chip (page 39).

11. Claims 9-11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos (US006136664A) in view of Van Zant (pages 31 and 39) and Schwalke (US 5,700,712).

Economikos teaches all of the positive steps of claims 9-11 and 17 except for the use of a substrate containing germanium and providing the conformal semiconductor layer by selective epitaxial growth.

Regarding claim 9, Economikos teaches a silicon substrate (column 4 line 10). The term "silicon substrate" generally refers to a substrate containing silicon, but is not limited to pure silicon. Van Zant teaches that silicon and germanium are both common substrate materials (page 31) giving them an art recognized equivalence for substrate material. Further, Van Zant teaches the use of silicon-germanium (strained layers) substrates as producing a faster chip (page 39).

Economikos teaches a mask (layers 10 and 15), selectively etching the mask (thus a photoresist and selectively removing portions of the photoresist, column 4 lines 5-6) layer to form apertures (45), forming trenches (47) at the location of the apertures by selectively etching the substrate, providing semiconductor material within the

trenches and forming an oxide liner using the semiconductor layer (column 4 lines 25-30) by an oxidation process (column 4 lines 25-26).

Economikos forms the conformal layer by deposition. Schwalke teaches forming the layer by deposition (column 5 line 11) or by selective epitaxial growth prior to oxidation (column 5 lines 34-35) giving the two methods an art recognized equivalence for forming the liner layer.

Regarding claim 10, Economikos teaches a pad oxide layer (10).

Regarding claim 11, the pad oxide is removed at the locations before forming the trench (column 4 lines 7-10, the pad oxide sits atop the substrate and must be removed first).

Regarding claim 17, Economikos teaches a silicon substrate (column 4 line 10). The term "silicon substrate" generally refers to a substrate containing silicon, but is not limited to pure silicon. Van Zant teaches that silicon and germanium are both common substrate materials (page 31) giving them an art recognized equivalence for substrate material. Further, Van Zant teaches the use of silicon-germanium (strained layers) substrates as producing a faster chip (page 39).

Economikos teaches a mask (layers 10 and 15), selectively etching the mask (thus a photoresist and selectively removing portions of the photoresist, column 4 lines 5-6) layer to form apertures (45), forming trenches (47) at the location of the apertures

by selectively etching the substrate, providing semiconductor material within the trenches and forming an oxide liner using the semiconductor layer (column 4 lines 25-30) by an oxidation process (column 4 lines 25-26).

Economikos forms the conformal layer by deposition. Schwalke teaches forming the layer by deposition (column 5 line 11) or by selective epitaxial growth prior to oxidation (column 5 lines 34-35) giving the two methods an art recognized equivalence for forming the liner layer.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Economikos to use a silicon-germanium substrate as taught by Van Zant to provide a faster chip (page 39) and to substitute selective epitaxial growth.for deposition as taught by Schwalke to have an art recognize equivalence.

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos (US006136664A) in view of Van Zant (pages 31 and 39) and Schwalke (US 5,700,712) and in further view of Vossen (page 333).

Economikos teaches all of the positive steps of claims 9-11 and 17 as recited above in regard to claim 17, except for epitaxial growth below 600C.

Regarding claim 18, Ecnonomikos and Schwalke teach the liner layer may be amorphous. Economikos deposits the layer below 600 degrees. Schwalke teaches epitaxy for crystal silicon at 800C. However, Vossen teaches that at temperature around 600C (and above), the films become monocrystalline (page 333) and amorphous silicon

may be grown at 500 degrees. Therefore it would be obvious for one skilled in the art to know that in order to form an amorphous film (by deposition or epitaxy) to form the film below 600 degrees.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos (US006136664A) in view of Van Zant (pages 31 and 39) and Schwalke (US 5,700,712) and in further view of Witek (US 6,146,970)

Economikos teaches all of the positive steps of claim 20 as recited above in regard to claim 17, except for the thickness of the oxide liner.

Witek teaches a liner should be 100-500A thick with 200A being optimal (column 7 lines 5-7) for complete silicon consumption.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Economikos to have a liner of 100-500A thick with 200A being optimal (column 7 lines 5-7) for complete silicon consumption.

14. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos (US006136664A) in view of Van Zant (pages 31 and 39) and in further view of Witek (US 6,146,970).

Economikos teaches all of the positive steps of claim 4 as recited above in regard to claim 1, except for an amorphous capping layer.

Economikos teaches a low temperature oxide layer above the substrate but does not teach an amorphous capping layer above the oxide. Witek teaches a capping layer of SiN or TEOS (TEOS is amorphous) above the oxide layer to protect the underlying bulk trench fill (column 8 lines 30-50).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Economikos to have teaches a capping layer of SiN or TEOS (TEOS is amorphous) above the oxide layer as taught by Witek to protect the underlying bulk trench fill (column 8 lines 30-50).

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos (US006136664A) in view of Van Zant (pages 31 and 39) and Schwalke (US 5,700,712) and in further view of Cho (GB 2 254 731 A).

Economikos teaches all of the positive steps of claim 12 as recited above in regard to claim 9, except for removing the hard mask in a wet bath.

Regarding claim 12, an insulative material (70) is placed in the trench and the hard mask is removed by planarization or RIE. Cho teaches removal of the silicon nitride hard mask by wet etching (a wet bath page 8 lines 15-17). As Cho was published in 1992, it is obvious that wet etching to remove a silicon nitride mask was well known at the time of the invention and one skilled in the requisite art would recognize the two as equivalent arts.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Economikos to remove the layer of SiN (hard mask) as taught to be well known by Cho and as such an art recognized equivalent.

16. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos (US006136664A) in view of Van Zant (pages 31 and 39) and Schwalke (US 5,700,712) and in further view of Vossen (pages 134 and 371).

Economikos teaches all of the positive steps of claim 19 except for providing the layer by molecular beam epitaxy (MBE). Economikos forms the conformal layer by deposition. Schwalke teaches forming the layer by deposition (column 5 line 11) or by selective epitaxial growth prior to oxidation (column 5 lines 34-35) giving the two methods an art recognized equivalence for forming the liner layer. Further, Vossen teaches that MBE is a form of selective epitaxial growth (page 371) and teaches MBE has the advantages of low growth temperature that limits diffusion and maintains hyperadrupt interfaces (page 134, 1 of 4 advantages listed).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Economikos and Schwalke to use MBE as taught by Vossen to have the advantages of low growth temperature that limits diffusion and maintains hyperadrupt interfaces (page 134, 1 of 4 advantages listed).

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

February 21, 2006